ZARLINK SEMICONDUCTOR

VoiceEdge

Le75181

Ringing Access Switch
VE750 Series

APPLICATIONS

- **Central office**
- **DLC**
- **PBX**
- **DAML**
- **HFC/FITL**

FEATURES

- **Small size/surface-mount packaging**
- **Monolithic IC reliability**
- **Low impulse noise**
- **Make-before-break, break-before-make operation**
- **Clean, bounce-free switching**
- **Low, matched ON-resistance**
- **Built-in current limiting, thermal shutdown, and SLIC protection**
- **5 V only operation, very low power consumption**
- **Battery monitor, all OFF state upon loss of battery**
- **No EMI**
- **Latched logic level inputs, no drive circuitry**
- **Only one external protector required**
- **TTL logic control compatible**
- **Default power up state**

RELATED LITERATURE

- **081123 Le75282 Dual Intelligent Line Card Access Switch Data Sheet**
- **081126 Le75183 Line Card Access Switch Data Sheet**
- **080754 Le58QL061/063 QLSLAC Data Sheet**
- **080676 Le5711 Dual SLIC Data Sheet**
- **081047 Le5712 Dual SLIC Data Sheet**

ORDERING INFORMATION

Device	Package Type[1]	Packing[2]
LE75181ABSC	16-Pin SOIC, GULL (Green)	Tube
LE75181BBSC		
LE75181CBSC		

1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

DESCRIPTION

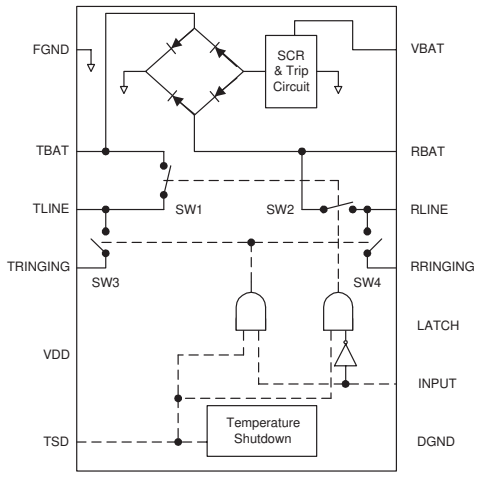
The VoiceEdge™ family VE750 series of Line Card Access Switches (LCAS) is a family of monolithic solid-state switches that is designed to provide both power ringing access and test access on the analog line card. These devices, while not a pin-for-pin replacement for the traditional electromechanical relay (EMR) solution, provide the equivalent switching functionality. The VE750 series LCAS is meant as a solid-state alternative to the EMRs.

The Le75181A/B device is pin-for-pin compatible with Zarlink's L7581A/B device, and the Le75181C device is pin-for-pin compatible with Zarlink's L8581A device.

Zarlink also offers a range of compatible SLIC devices and codec/filters that can be used with the VE750 series LCAS for complete line card solutions that can be used worldwide in analog line card applications.

BLOCK DIAGRAM

Le75181A/C



Le75181B

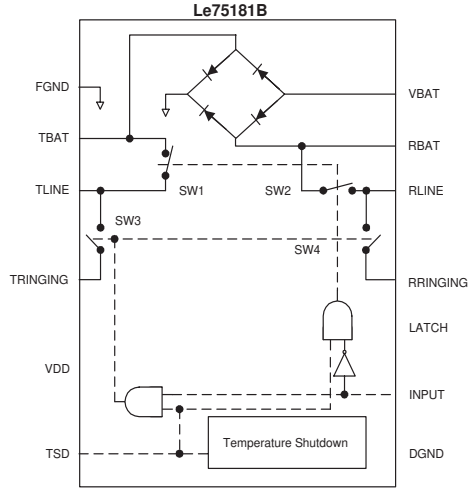


TABLE OF CONTENTS

PRODUCT DESCRIPTION

The Le75181 Ringing Access Switch is a monolithic solid-state device that provides the switching functionality of a two-form C switch.

The Le75181 is designed to provide power ringing access to tip and ring in central office, digital loop carrier, private branch exchange, digitally added main line, and hybrid fiber coax/fiber-in-the-loop analog line card applications. The Le75181 has three states: the idle talk state (line break switches closed, ringing access switches open), power ringing state (line break switches open, ringing access switches closed), and all OFF state.

The Le75181 offers break-before-make or make-before-break switching, with simple logic level input control. Because of the solid-state construction, voltage transients generated when switching into an inductive ringing load during ring cadence or ring trip are minimized, possibly eliminating the need for external zero cross switching circuitry. State control is via logic level inputs, so no additional driver circuitry is required.

The line break switch is a linear switch that has exceptionally low ON-resistance and an excellent ON-resistance matching characteristic. The ringing access switch has a breakdown voltage rating >480 V which is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ringing generator).

Incorporated into the Le75181A and Le75181C is a diode bridge/SCR clamping circuit, current-limiting circuitry, and a thermal shutdown mechanism to provide protection to the SLIC device and subsequent circuitry during fault conditions (see block diagram). Positive and negative lightning is reduced by the current-limiting circuitry and steered to ground via diodes and the integrated SCR. Power cross is also reduced by the current-limiting and thermal shutdown circuits.

The Le75181B version provides only an integrated diode bridge along with current limiting and thermal shutdown, as shown in the block diagram. This will cause positive faults to be directed to ground and negative faults to battery. In either polarity, faults are reduced by the current-limit and/or thermal shutdown mechanisms.

The default power up state is in Idle/Talk state unless otherwise being overwritten by external controls.

To protect the Le75181 from an overvoltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the tip/ring terminals to prevent the breakdown voltage of the switches from being exceeded. To minimize stress on the solid-state contacts, use of a foldback- or crowbar- type secondary protector is recommended. With proper choice of secondary protection, a line card using the Le75181 will meet all relevant ITU-T, LSSGR, FCC, or UL* protection requirements.

The Le75181 operates off of a 5-V supply only. This gives the device extremely low idle and active power dissipation and allows use with virtually any range of battery voltage. This makes the Le75181 especially appropriate for remote power applications such as DAML or FOC/FITL or other Bellcore TA 909 applications where power dissipation is particularly critical.

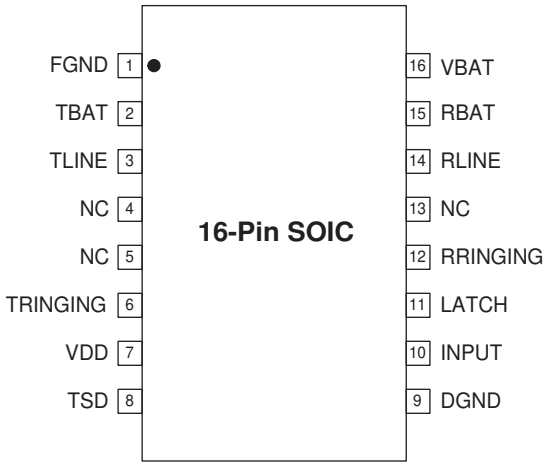
A battery voltage is also used by the Le75181, only as a reference for the integrated protection circuit. The Le75181 will enter an all OFF state upon loss of battery.

During power ringing, to turn on and maintain the ON state, the ring access switch will draw a nominal 2 mA from the ring generator.

The Le75181ASC/BSC/CSC device is packaged in a 16-pin, plastic SOIC (GULL) package.

CONNECTION DIAGRAMS

Figure 1. 16-Pin SOIC



Pin Descriptions

Pin Name	Type	Description
DGND	Ground	Digital ground.
FGND	Ground	Fault ground.
INPUT	Input	Logic level input switch control. Internally 75 kΩ typical pull down.
LATCH	Input	Data latch control, active-high, transparent low. Internally 75 kΩ typical pull down.
NC	—	No connection.
RBAT	Input/Output	Connect to RING on SLIC side.
RLINE	Input/Output	Connect to RING on line side.
RRINGING	Input/Output	Connect to ringing generator.
TBAT	Input/Output	Connect to TIP on SLIC side.
TLINE	Input/Output	Connect to TIP on line side.
TRINGING	Input/Output	Connect to return ground for ringing generator.
TSD	Input/Output	Temperature shutdown pin. Can be used as a logic level input or output. See table 8, truth table, on page 15, and the Switching Behavior section of this data sheet for input pin description. As an output, will read HIGH when device is in its operational mode and LOW in the thermal shutdown mode. In the Le75181, the thermal shutdown mechanism cannot be disabled.
VBAT	Input	Battery voltage. Used as a reference for protection circuit.
VDD	Power	5-V supply.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Min	Max	Unit
Operating Temperature Range	–40	110	°C
Storage Temperature Range	–40	150	°C
Relative Humidity Range	5	95	%
Pin Soldering Temperature (t=10 s max)	—	260	°C
5-V Power Supply	-0.3	7	V
Battery Supply	—	–85	V
Logic Input Voltage	-0.3	V_{DD}+0.3	V
Input-to-output Isolation	—	330	V
Pole-to-pole Isolation (All except SW 4)	—	330	V
Pole-to-pole Isolation (Ringing Access Switch, SW4)	—	480	V
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant		

Package Assembly

Green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Environmental Ranges

Zarlink guarantees the performance of this device over commercial (0 to 70º C) and industrial (-40 to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Ambient Temperature	–40° to 85°C

Electrical Ranges

Supply	Min	Typ	Max	Unit
V_{DD}	4.5	5	5.5	V
V_{BAT}*	–19	—	–72	

**V_{BAT} is used only as a reference for internal protection circuitry. If V_{BAT} rises above –10 V, the device will enter an all OFF state and remain in this state until the battery voltage drops below –15 V.*

ELECTRICAL CHARACTERISTICS

Summary of Assumptions

Unless otherwise noted, the test conditions are defined by the Le75181 device application circuit shown in Figure 7. on page 14 with:

V_{BAT} = –48 V, V_{DD} = 5.0 V.

Supply Currents and Power Dissipation

Operational State	Condition	I_{DD} mA			I_{BAT} µA			LCAS Device Power mW		
		Min.	Typ	Max	Min.	Typ	Max	Min.	Typ	Max
Power Ringing	VDD=5V, VBAT=-48V	—	0.850	2.1	—	4	10	—	6	11
Idle/Talk	VDD=5V, VBAT=-48V	—	0.560	1.1	—	4	10	—	3	6

SPECIFICATIONS

Device Specifications

Table 1. Break Switches, 1 and 2

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current:						µA
+25 °C	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 V to +260 V	Iswitch	—	—	1	
+85 °C	Vswitch (differential) = –330 V to Gnd Vswitch (differential) = –60 V to +270 V	Iswitch	—	—	1	
–40 °C	Vswitch (differential) = –310 V to Gnd Vswitch (differential) = –60 V to +250 V	Iswitch	—	—	1	
ON-resistance (SW1, SW2):						Ω
+25 °C	TLINE = ±10 mA, ±40 mA, TBAT = –2 V	Δ VON	—	21.5	—	
+85 °C	TLINE = ±10 mA, ±40 mA, TBAT = –2 V	Δ VON	—	—	31	
–40 °C	TLINE = ±10 mA, ±40 mA, TBAT = –2 V	Δ VON	—	16	—	
ON-resistance Match	Per ON-resistance test condition of SW1, SW2	Magnitude RON SW1 – RON SW2	—	0.2	1.0	Ω
ON-state Voltage* (Figure 5, Switch 1)	Iswitch = ILIMIT @ 50 Hz/60 Hz	VON	—	—	220	V
ON-state Voltage* (Figure 6, Switch 2)	Maximum Differential Voltage (Vmax)	VON	—	—	320	V
	Foldback Voltage Breakpoint 1 (V1)	VON	100	—	—	
	Foldback Voltage Breakpoint 2 (V2)	VON	V1+0.5	—	—	
dc Current Limit (Figure 5, Switch 1):						mA
+85 °C	Vswitch (on) = ±10 V	Iswitch	80	—	—	
–40 °C	Vswitch (on) = ±10 V	Iswitch	—	—	250	
dc Current Limit (Figure 6, Switch 2):	I_{LIMIT1}	Iswitch	80	—	250	mA
	I_{LIMIT2}	Iswitch	1	—	—	
Dynamic Current Limit (t = <0.5 µs)	Break switches in ON state; ringing access switches off; apply ±1000 V at 10/1000 µs pulse; appropriate secondary protection in place	Iswitch	—	2.5	—	A
Isolation:						µA
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd	Iswitch	—	—	1	
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd	Iswitch	—	—	1	
dV/dt Sensitivity†	—	—	—	200	—	V/µs

**This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

†Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.

Table 2. Ring Return Switch, 3

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current (SW3):						
+25 °C	Vswitch (differential) = –320 V to Gnd Vswitch (differential) = –60 V to +260 V	Iswitch	—	—	1	µA
+85 °C	Vswitch (differential) = –330 V to Gnd Vswitch (differential) = –60 V to +270 V	Iswitch	—	—	1	
–40 °C	Vswitch (differential) = –310 V to Gnd Vswitch (differential) = –60 V to +250 V	Iswitch	—	—	1	
dc Current Limit	Vswitch (on) = ±10 V	Iswitch	—	200	—	mA
ON-resistance	Iswitch (on) = 0 mA, ±10 mA	Δ VON	—	—	100	Ω
ON-state Voltage*	Iswitch = ILIMIT @ 50 Hz/60 Hz	VON	—	—	130	V
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd	Iswitch	—	—	1	µA
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd	Iswitch	—	—	1	
dV/dt Sensitivity†	—	—	—	200	—	V/µs

**This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

†Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.

Table 3. Ringing Access Switch, 4

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
OFF-state Leakage Current (SW3):						
+25 °C	Vswitch (differential) = –255 V to +210 V Vswitch (differential) = +255 V to –210 V	Iswitch	—	—	1	µA
+85 °C	Vswitch (differential) = –270 V to +210 V Vswitch (differential) = +270 V to –210 V	Iswitch	—	—	1	
–40 °C	Vswitch (differential) = –245 V to +210 V Vswitch (differential) = +245 V to –210 V	Iswitch	—	—	1	
ON-resistance	Iswitch (on) = ±70 mA, ±80 mA	Δ VON	—	—	12	Ω
ON Voltage	Iswitch (on) = ± 1 mA	—	—	—	3	V
Ring Generator Current During Ring	VCC = 5 V INPUT = 1	IRINGSOURCE	—	2	—	mA
Steady-state Current†	—	—	—	—	150	mA
Surge Current†	—	—	—	—	2	A
Release Current	—	—	—	500	—	µA
Isolation:						
+25 °C	Vswitch (both poles) = ±320 V, Logic inputs = Gnd	Iswitch	—	—	1	µA
+85 °C	Vswitch (both poles) = ±330 V, Logic inputs = Gnd	Iswitch	—	—	1	
–40 °C	Vswitch (both poles) = ±310 V, Logic inputs = Gnd	Iswitch	—	—	1	
dV/dt Sensitivity‡	—	—	—	200	—	V/µs

**This parameter is not tested in production. Choice of secondary protector should ensure this rating is not exceeded.*

†Applied voltage is 100 Vp-p square wave at 100 Hz. Not tested in production.

Table 4. Additional Electrical Characteristics

Parameter	Test Condition	Measure	Min	Typ	Max	Unit
Digital Input Characteristics						
Input Low Voltage	—	—	—	—	0.8	V
Input High Voltage	—	—	2.2	—	—	V
Input Leakage Current (high)	V_{DD} = 5.5 V, V_{BAT} = –75 V, Vlogicin = 5 V	Ilogicin	—	—	500	µA
Input Leakage Current (low)	V_{DD} = 5.5 V, V_{BAT} = –75 V, Vlogicin = 0 V	Ilogicin	—	—	500	µA
Input Leakage Current (high) INPUT, LATCH	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 5 V	Ilogicin	—	100	—	µA
Input Leakage Current (low) INPUT, LATCH	V_{DD} = 5.5 V, V_{BAT} = –58 V, Vlogicin = 0 V	Ilogicin	—	0.5	—	µA
Input Current (Sourcing from LCAS) (low) TSD	V_{DD} = 5.5 V, V_{BAT} = –58 V, V_{TSD} = 0 V	I_{TSD}	0.5	1.0	2.0	mA
Temperature Shutdown Requirements*						
Shutdown Activation Temperature	—	—	110	125	150	°C
Shutdown Circuit Hysteresis	—	—	10	—	25	°C

**Temperature shutdown flag (TSD) will be high during normal operation and low during temperature shutdown state.*

ZERO CROSS CURRENT TURN OFF

The ring access switch (SW4) is designed to turn off on the next zero current crossing after application of the appropriate logic input control. This switch requires a current zero cross to turn off. Switch 4, once on, will remain in the ON state (regardless of logic input) until a current zero cross. Therefore, to ensure proper operation of switch 4, this switch should be connected, via proper impedance, to the ringing generator or some other ac source. Do not attempt to switch pure DC with switch 4.

For a detailed explanation of the operation of switch 4, please refer to the *An Introduction to Le758X Series of Line Card Access Switches* application note.

SWITCHING BEHAVIOR

When switching from the Power Ringing state to the Idle/Talk state via simple logic level input control, the Le75181 is able to provide control with respect to the timing when the ringing access contacts are released relative to the state of the line break contacts.

Make-before-break operation occurs when the line break switch contacts are closed (or made) before the ringing access switch contact is opened (or broken). Break-before-make operation occurs when the ringing access contact is opened (broke) before the line break switch contacts are closed (made).

Using the logic level input pins INPUT and TSD, either make-before-break or break-before-make operation of the Le75181 is easily achieved. The logic sequences for either mode of operation are given in Table 5 and Table 6. See Table 8, *Truth Table*, on page 14 for an explanation of the logic states.

When using an Le75181 device in the make-before-break mode, during the ring-to-idle transition, for a period of up to one-half the ringing frequency, the ring break switch and the pnpn-type ring access switch can both be in the ON state. This is the maximum time after the logic signal at IN_{RING} has transitioned that the ring access switch is waiting for the next zero current cross so it can close. During this interval, current that is limited to the dc break switch current-limit value will be sourced from the ring node of the SLIC device.

This current is presented to the internal protection circuit. If the SCR-type protector is used (A/C codes), if by random probability the ring-to-idle transition occurs during a portion of the ring cycle when the ringing voltage exceeds the protection circuit SCR turn-on voltage, and if current in excess of the SCR's turn-on current is also available, the SCR may turn on. Once the SCR is triggered on, if the SLIC device is capable of supplying current in excess of the holding current, the SCR may be latched on by the SLIC device.

The probability of this event depends on the characteristics of the given SLIC device and of the holding current of the Le75181A/C devices. The SCR hold current distribution is designed to be safely away from the test limit of 80 mA for Le75181A device. The limit for Le75181C device is 110 mA. The higher the distribution, the lower the probability of the latch.

If this situation is of concern for a given board design, either use the A/C series device in the break-before-make mode (eliminates the original 25 ms current pulse) or use a B series device (eliminates the SCR).

Table 5. Make-Before-Break Operation

INPUT	TSD	State	Timing	Break Switches 1 & 2	Ring Return Switch 3	Ring Access Switch 4
1	1/Float	Power Ringing	—	Open	Closed	Closed
0	1/Float	Make-before-break	SW4 waiting for next zero current crossing to turn off, maximum time—one-half of ringing. In this transition state, current that is limited to the dc break switch current-limit value will be sourced from the ring node of the SLIC.	Closed	Open	Closed
0	1/Float	Idle/Talk	Zero cross current has occurred.	Closed	Open	Open

Table 6. Break-Before-Make Operation

INPUT	TSD	State	Timing	Break Switches 1 & 2	Ring Return Switch 3	Ring Access Switch 4
1	1/Float	Power Ringing	—	Open	Closed	Closed
1	0	All Off	Hold this state for ≤25 ms. SW4 waiting for zero current to turn off.	Open	Open	Closed
0	0	All Off	Zero current has occurred and SW4 has opened. Transition on INPUT should occur during 25 ms hold.	Open	Open	Open
0	1/Float	Idle/Talk	Release break switch pair.	Closed	Open	Open

POWER SUPPLIES

Though both the 5-V and battery supplies are brought onto the Le75181 device, only the 5-V supply is required for switch operation; that is, state control is powered exclusively off of the 5-V supply. Because of this, the Le75181 device offers extremely low power dissipation, both in the Idle and Active states.

The battery voltage is not used for switch state control, but rather as a reference voltage by the integrated secondary protection circuit. When the voltage at TBAT or RBAT drops 2 V to 4 V below the battery, the integrated SCR will trigger, thus preventing fault-induced overvoltage situations at the TBAT/RBAT nodes.

LOSS OF BATTERY VOLTAGE

As an additional protection feature, the Le75181 device monitors the battery voltage. Upon loss of battery voltage, the Le75181 will automatically enter an all OFF state and remain in that state until the battery voltage is restored. The Le75181 is designed so that the device will enter the all OFF state if the battery rises above approximately –10 V and will remain off until the battery drops below approximately –15 V.

Monitoring the battery for the automatic shutdown feature will draw a small current from the battery, typically 4 µA. This will add slightly to the overall power dissipation of the device.

IMPULSE NOISE

Using the Le75181 will minimize and possibly eliminate the contribution to the overall system impulse noise that is associated with ringing access switches. Because of this characteristics of the Le75181, it may not be necessary to incorporate a zero cross switching scheme. This ultimately depends upon the characteristics of the individual system and is best evaluated at the board level.

PROTECTION

Integrated SLIC Device Protection

Diode Bridge/SCR

In the Le75181A/C version, protection to the SLIC device or other subsequent circuitry is provided by a combination of current-limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism. In the Le75181B version, protection to the SLIC device or other subsequent circuitry is provided by a combination of current-limited break switches, a diode bridge, and a thermal shutdown mechanism.

In both versions, during a positive lightning event, fault current is directed to ground via steering diodes in the diode bridge. Voltage is clamped to a diode drop above ground. In the A/C versions, negative lightning causes the SCR to conduct when the voltage goes 2 V to 4 V more negative than the battery, and fault currents are directed to ground via the SCR and steering diodes in the diode bridge.

Note that for the SCR to foldback or crowbar, the ON voltage (see Table 7) of the SCR must be less negative than the battery reference voltage. If the battery voltage is less negative than the SCR ON voltage, the SCR will conduct fault currents to ground; however, it will not crowbar.

In the B version, negative lightning is directed to battery via steering diodes in the diode bridge.

For power cross and power induction faults, in both versions, the positive cycle of the fault is clamped a diode drop above ground and fault currents steered to ground. In the A/C versions, the negative cycle will cause the SCR to trigger when the voltage exceeds the battery reference voltage by 2 V to 4 V. When the SCR triggers, fault current is steered to ground. In the B version, the negative cycle of the power cross is steered to battery.

Current Limiting

During a lightning event, the current that is passed through the break switches and presented to the integrated protection circuit and subsequent circuitry is limited by the dynamic current-limit response of the break switches (assuming idle/talk state). When the voltage seen at the TLINE/RLINE nodes is properly clamped by an external secondary protector, upon application of a 1000 V 10 x 1000 pulse (LSSGR lightning), the current seen at the TBAT/RBAT nodes will typically be a pulse of magnitude 2.5 A and duration less than 0.5 µs.

During a power cross event, the current that is passed through the break switches and presented to the integrated protection circuit and subsequent circuitry is limited by the dc current-limit response of the break switches (assuming idle/talk state). The DC current limit is specified over temperature between 80 mA and 250 mA.

Note that the current-limit circuitry has a negative temperature coefficient. Thus, if the device is subjected to an extended power cross, the value of current seen at TBAT/RBAT will decrease as the device heats due to the fault current. If sufficient heating occurs, the temperature shutdown mechanism will activate and the device will enter an all off mode.

Temperature Shutdown Mechanism

When the device temperature reaches a minimum of 110°C, the thermal shutdown mechanism will activate and force the device into an all OFF state, regardless of the logic input pins. Pin TSD, when used as an output, will read LOW when the device is in the thermal shutdown mode and HIGH during normal operation.

During a lightning event, due to the relatively short duration, the thermal shutdown will not typically activate.

During an extended power cross, the device temperature will rise and cause the device to enter the thermal shutdown mode. This forces an all off mode, and the current seen at TBAT/RBAT drops to zero. Once in the thermal shutdown mode, the device will cool and exit the thermal shutdown mode, thus reentering the state it was in prior to thermal shutdown. Current, limited to the dc current-limit value, will again begin to flow and device heating will begin again. This cycle of entering and exiting thermal shutdown will last as long as the power cross fault is present. The frequency of entering and exiting thermal shutdown will depend on the magnitude of the power cross.

If the magnitude of the power cross is great enough, the external secondary protector may trigger shunting all current to ground.

In the Le75181 device, the thermal shutdown mechanism cannot be disabled by logic control at the TSD pin. The functionality of TSD differs from the Le75282 and Le75183 devices. For the proper use of and understanding of any caveats related to TSD, please refer to the appropriate data sheet specifications.

Electrical specifications relating to the overvoltage clamping circuit are outlined in Table 7.

External Secondary Protector

With the above integrated protection features, only one overvoltage secondary protection device on the loop side of the Le75181 device is required. The purpose of this device is to limit fault voltages seen by the Le75181 device so as not to exceed the breakdown voltage or input-output isolation rating of the device. To minimize stress on the Le75181 device, use of a foldback- or crowbar-type device is recommended. A detailed explanation and design equations on the choice of the external secondary

protection device are given in the *An Introduction to Le758X Series of Line Card Access Switches* application note. Basic design equations governing the choice of external secondary protector are given below:

- $|V_{BATmax}| + |V_{breakovermax}| < |V_{breakdownmin(break)}|$
- $|V_{ringingpeakmax}| + |V_{BATmax}| + |V_{breakovermax}| < |V_{breakdownmin(ring)}|$
- $|V_{ringingpeakmax}| + |V_{BATmax}| < |V_{breakovermin}|$

where:

V_{BATmax}—Maximum magnitude of battery voltage.

$V_{breakovermax}$—Maximum magnitude breakover voltage of external secondary protector.

$V_{breakovermin}$—Minimum magnitude breakover voltage of external secondary protector.

$V_{breakdownmin(break)}$—Minimum magnitude breakdown voltage of Le75181 break switch.

$V_{breakdownmin(ring)}$—Minimum magnitude breakdown voltage of Le75181 ring access switch.

$V_{ringingpeakmax}$—Maximum magnitude peak voltage of ringing signal.

Series current-limiting fused resistors or PTC resistors should be chosen so as not to exceed the current rating of the external secondary protector. Refer to the manufacturer's data sheet for specifications.

Table 7. Electrical Specifications, Protection Circuitry

Parameters Related to Diodes (in Diode Bridge)						
Parameter	**Test Condition**	**Measure**	**Min**	**Typ**	**Max**	**Unit**
Voltage Drop at Continuous Current (50 Hz/60 Hz)	Apply ±dc current limit of break switches	Forward Voltage	—	—	3.5	V
Voltage Drop at Surge Current	Apply ±dynamic current limit of break switches	Forward Voltage	—	5	—	V
Parameters Related to Protection SCR						
Surge Current	—	—	—	—	‡	A
Gate Trigger Current (Le75181A)*†	—	—	—	25	50	mA
Gate Trigger Current (Le75181C)*†	—	—	—	33	70	mA
Gate Trigger Current† Temperature Coefficient	—	—	—	–0.5	—	%/°C
Hold Current (Le75181A)	—	—	70	—		mA
Hold Current (Le75181C)	—	—	110	—		mA
Gate Trigger Voltage	Trigger current	—	VBAT – 4	—	VBAT – 2	V
Reverse Leakage Current	VBAT	—	—	—	1.0	µA
ON-State Voltage§	0.5 A, t = 0.5 µs 2.0 A, t = 0.5 µs	V_{ON} —	— —	–3 –5	— —	V V

** Trigger Current is defined as the minimum current drawn from tip and ring to turn on the SCR. The specification in this data sheet is Gate Trigger Current, which is defined as the maximum current that can flow into the battery before the SCR turns on.*

† Typical at 25 °C

‡ Twice ± dynamic current limit of break switches.

§ In some instances, the typical ON-state voltage can range as low as –25 V.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 2. Protection Circuit A/C Version

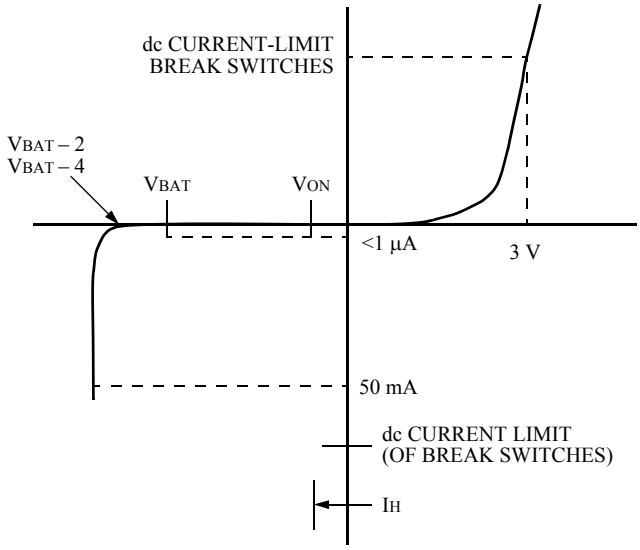


Figure 3. Protection Circuit B Version

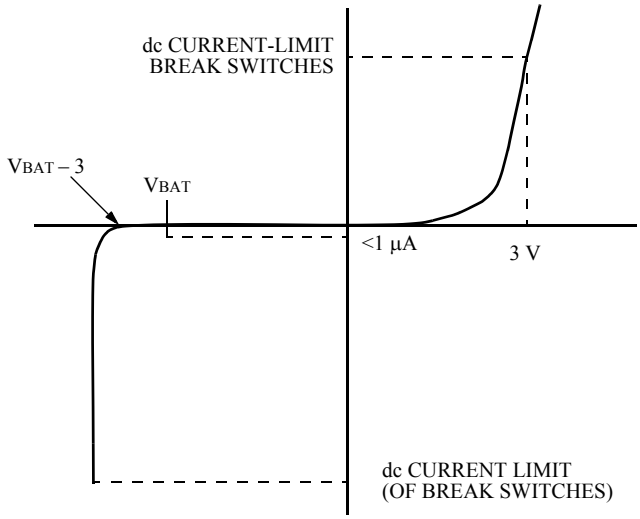


Figure 4. Switches 1 and 3

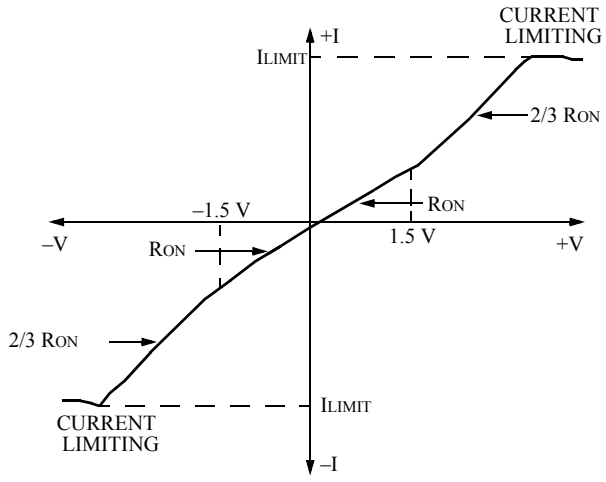


Figure 5. Switch 2

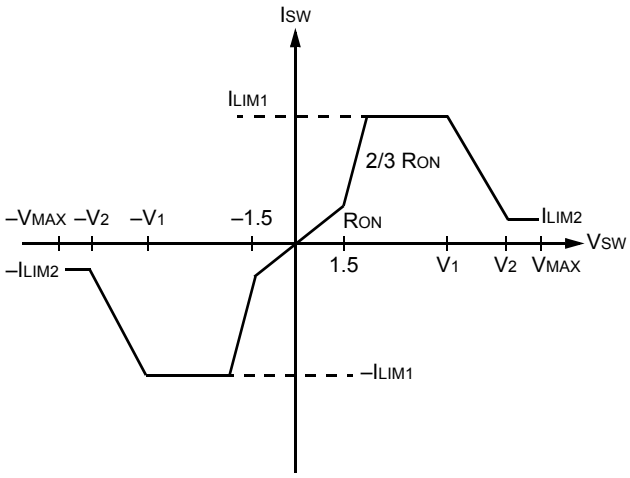
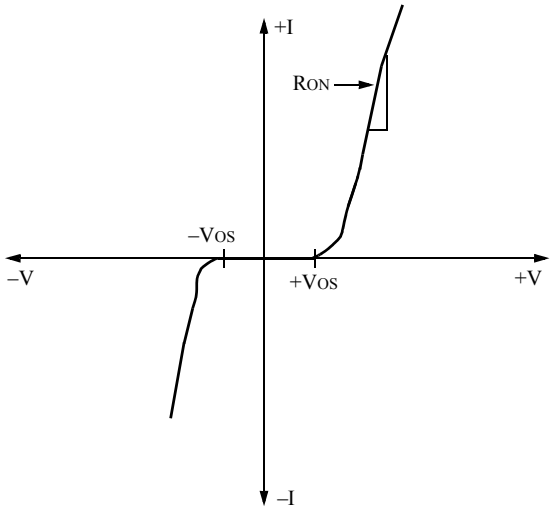
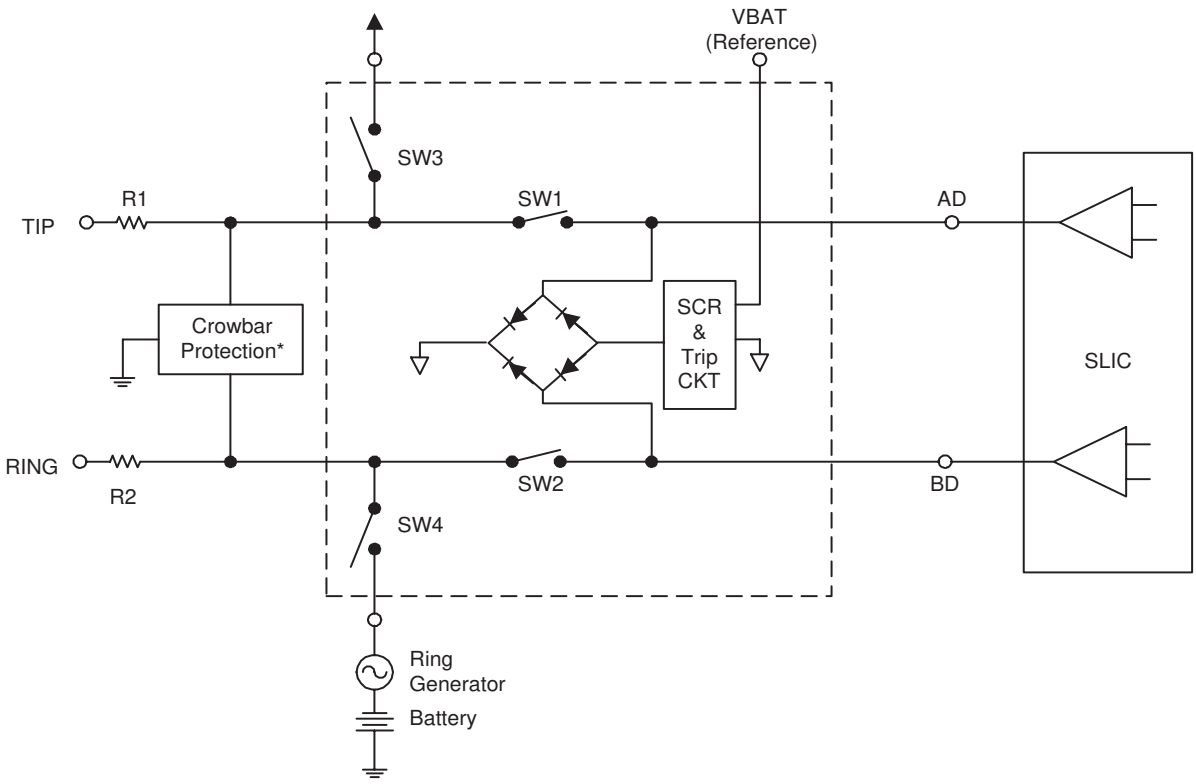


Figure 6. Switch 4



APPLICATION

Figure 7. Typical LCAS Application, A/C Versions, Idle or Talk State Shown



**Contact a Zarlink Sales/Application representative for recommendations.*

Table 8. Truth Table

INPUT	TSD	Tip Break Switch	Ring Break Switch	Ringing Return Switch	Ring Switch
0	1/Float[1]	Closed	Closed	Open	Open[3, 6]
1	1/Float[1]	Open	Open	Closed	Closed[4]
Don't Care	0	Open	Open	Open	Open[5]

1. *Thermal shutdown mechanism is active with TSD floating or HIGH.*
2. *Forcing TSD to LOW overrides the logic input pins and forces an all OFF state.*
3. *Idle/Talk state.*
4. *Power ringing state.*
5. *All OFF state.*
6. *Default power up state.*

A parallel in/parallel out data latch is integrated into the Le75181 device. Operation of the data latch is controlled by the logic level input pin LATCH. The data input to the latch is the INPUT pin of the Le75181 device, and the output of the data latch is an internal node used for state control.

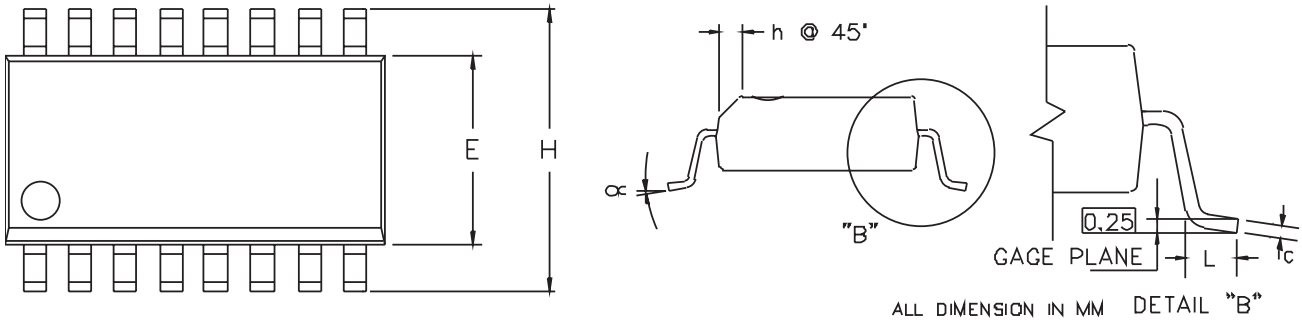
When the LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly from INPUT, through the data latch to state control. Any changes in INPUT will be reflected in the state of the switches.

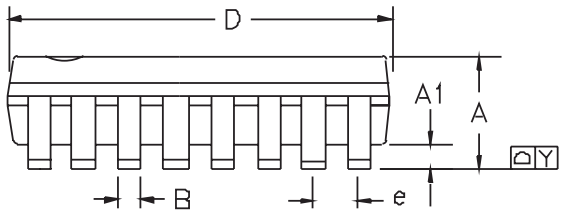
When the LATCH control pin is at logic 1, the data latch is active—the Le75181 device will no longer react to changes at the INPUT control pin. The state of the switches is now latched; that is, the state of the switches will remain as they were when the LATCH input transitioned from logic 0 to logic 1. The switches will not respond to changes in INPUT as long as LATCH is held high.

Note that the TSD input is not tied to the data latch. TSD is not affected by the LATCH input. TSD input will override state control via INPUT and LATCH.

PHYSICAL DIMENSIONS

16-Pin, Plastic SOIC (GULL) (ASC/BSC/CSC)





Small Outline Package (16 SOIC)						
Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A	2.35	2.54	2.65	0.092	0.100	0.104
A1	0.10	0.17	0.30	0.004	0.006	0.012
B	0.33	0.42	0.51	0.013	0.016	0.020
C	0.23	0.25	0.32	0.009	0.010	0.012
E	7.40	7.50	7.60	0.291	0.295	0.299
e	1.27 BSC			0.050 BSC		
H	10.00	10.30	10.65	0.394	0.406	0.419
h	0.25	0.50	0.75	0.009	0.020	0.029
L	0.40	0.70	1.27	0.015	0.028	0.050
	0 deg	-	8 deg	0 deg	-	8 deg
Y	0.00		0.01	0.000	-	0.004
D	10.10	10.31	10.50	0.398	0.406	0.413

16-Pin SOIC

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision A1 to B1

- Page 1, changed OPNs from Le75181xx to Le75181xxC.
- Page 3, towards the end, changed Le75181xx to Le75181xxC.
- Page 16, changed Le75181xS to Le75181xSC.
- Page 17, changed Le75181xQ to Le75181xQC.
- Page 17, updated drawing for QFN package by adding line brakes.

Revision B1 to C1

- Removed QFN packaging information
- Page 8, Table 4, added TSD sourcing current specification

Revision C1 to D1

- Added green package OPNs to *Ordering Information*, on page 1
- Added *Package Assembly*, on page 5

Revision D1 to E1

- Removed non-green OPNs from *Ordering Information*, on page 1
- Added notes to *Ordering Information*, on page 1

Revision E1 to E2

- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

For more information about all Zarlink products visit our Web Site at

www.zarlink.com